What is claimed is:

1. A push-pull driver circuit, comprising:

an NMOS output transistor and PMOS output transistor connected between a voltage source and ground, wherein the respective drains of the NMOS and PMOS output transistors are commonly connected to a driver circuit output terminal;

an NMOS pre-driver transistor driving the NMOS output transistor in response to a transmit signal being applied to the NMOS pre-driver transistor through a drive signal path;

a non-overlap circuit defining a non-overlap signal path for the transmit signal being applied to the NMOS pre-driver transistor; and

wherein the delay through the non-overlap signal path is less than the delay through the drive signal path.

2. The push-pull driver circuit of claim 1, further comprising:

a boot-strap circuit defining a boot-strap signal path for the transmit signal being applied to the NMOS pre-driver transistor, wherein the delay through the boot-strap path is greater than the delay through the non-overlap signal path and less than the delay through the drive signal path.

3. The push-pull driver of claim 2, wherein the boot-strap circuit comprises:

a gate detecting an output voltage at the driver circuit output terminal and generating a charge pump enable signal;

a charge pump circuit applying charge to the NMOS pre-driver transistor in response to the charge pump enable signal.

4. The push-pull driver of claim 3, wherein the charge pump circuit comprises a positive feedback loop.

5. The push-pull driver of claim 1, further comprising:

a circuit for disabling the PMOS output transistor.

6. A circuit comprising:

a push-pull output driver having an output driver current path comprising a NMOS drive transistor and a PMOS drive transistor connected between a voltage source and ground, and also having an output driver reference element;

a process detector having a process detector reference element and providing at least one control signal defining a switching signal for the push-pull output driver;

a feedback circuit indicating current shoot-through occurring in the push-pull output driver and providing a feedback control signal; and,

a control circuit receiving the at least one control signal and modifying the switching signal in response to the feedback control signal;

wherein the output driver reference element and the process detector element respond similarly to variations in fabrication processes for the circuit, as well as operating temperature and operating voltage.

7. The circuit of claim 6, wherein the process detector comprises a delay lock loop (DLL) and the at least one control signal comprises digital codes derived from the DLL.

8. The circuit of claim 7 further comprising:

an adjustment circuit receiving the digital control codes;

separate P and N data registers respectively storing P control codes and N control codes;

a first digital to analog (D/A) converter receiving the P control codes and generating an analog P bias signal;

a second D/A converter receiving the N control codes and generating an analog N bias signal; and,

a pre-driver circuit comprising a NMOS pre-driver transistor receiving the N bias signal and a CMOS pre-driver transistor receiving the P bias signal.

9. The circuit of claim 7, wherein the feedback circuit comprises:

a mirrored output driver current path comprising a NMOS mirror transistor and a PMOS mirror transistor;

resistors converting a current output from the NMOS mirror transistor into an N feedback voltage and a current output from the PMOS mirror transistor into a P feedback voltage;

a XOR gate receiving the N feedback voltage and the P feedback voltage and generating a shoot-through flag when shoot-through is indicated in the mirrored output driver current path.

10. The circuit of claim 9, wherein the control circuit comprises:

latch circuits capturing shoot-through flags from the XOR gate and providing a pumpup signal to control logic storing a copy of the digital control codes;

wherein the control logic defining a shoot-through detection cycle and resetting the latch circuits following each shoot-through detection cycle.

11. A method of defining performance in a push-pull driver circuit having an output driver current path comprising a first output transistor and a second output transistor connected between a voltage source and ground, the method comprising:

defining a transmission switching signal for the first and second output transistors;

detecting shoot-through in the output driver current path;

generating a feedback signal in response to a detection of shoot-through in the output driver current path; and,

modifying the transmission switching signal in response to the feedback signal.

12. The method of claim 11, wherein the transmission switching signal comprises a first switching signal applied to the first output transistor and a second switching signal applied to the second output transistor.

13. The method of claim 12, wherein the step of modifying the transmission switching signal comprises adjusting the duty cycle of at least one of the first and second switching signals.

14. The method of claim 12, wherein the step of modifying the transmission switching signal comprises adjusting modifying a delay between the first and second switching signals.

15. The method of claim 1, wherein the push-pull driver further comprises a driver mirror current path arranged in parallel with the output driver current path, the driver mirror current path comprising a first mirror transistor sized in relation to the first output transistor and a second mirror transistor sized in relation to the second output transistor, and wherein the step of detecting shoot-through in the output driver current path comprises:

detecting mirrored shoot-though current in the driver mirror current path.

16. The method of claim 15, further comprising:

converting the mirrored shoot-though current into a shoot-through detection voltage, wherein the feedback signal is derived from the shoot-through detection voltage.

17. The method of claim 16, wherein the step of defining a transmission switching signal for the first and second output transistors comprises; defining control codes in a process detector having at least one process detector reference element, wherein the control codes determine the transmission switching signal for the first and second output transistors;

wherein the step of modifying the transmission switching signal in response to the feedback signal comprises; incrementing the control codes in response to the feedback signal; and

wherein at least one of the first and second output transistors comprises an output driver reference element that tracks performance of the process detector element over a range of variations in fabrication process, operating temperature, and operating voltage.

18. An output driver circuit, comprising:

a PMOS output transistor having a source connected to a voltage source and a drain connected to an output terminal;

a NMOS output transistor having source connected to ground and a drain connected to the output terminal;

a pre-driver circuit operable in one of two modes, the first mode applying a transmit signal to the PMOS output transistor and the NMOS output transistor to form a push-pull output driver circuit, and the second mode applying the transmit signal to only the NMOS output transistor to form an open-gate NMOS driver circuit.

19. The output driver of claim 18, further comprising:

a boot-strap circuit increasing enhancing the rising edge of an output signal in both the first and second modes; and

a non-overlap circuit being enabled in the first mode and disabled in the second mode.

20. A method of defining performance in a push-pull driver comprising a first output transistor and a second output transistor and an output driver current path between the first and second output transistors, the method comprising:

defining digital control codes in relation to a process detector, wherein the process detector exhibits performance characteristics which track the performance characteristics of the first and second output transistors;

defining a transmission switching signal for at least one of the first and second output transistors in relation to the digital control codes;

detecting shoot-through in the output driver current path;

generating a feedback signal in response to a detection of shoot-through in the driver current path;

modifying the digital control codes in response to the feedback signal.

21. The method of claim 20, wherein the process detector comprises a Delay Lock Loop circuit having performance characteristics that track the performance characteristics of the first and second output transistors in relation to at least one of process, voltage, and temperature.

22. A method of controlling shoot-through current in a push-pull driver circuit, comprising:

defining a transmission switching signal for the push-pull driver circuit in relation to a control signal received from a process detector;

adjusting the control signal and thereby modifying the transmission switching signal until a shoot-through crossover point is determined at which no shoot-through current occurs in the push-pull driver circuit;

upon determining the shoot-through crossover point, periodically dithering the control signal to re-introduce shoot-through current;

following re-introduction of shoot-through current, adjusting the control signal and thereby modifying the transmission switching signal until a new shoot-through crossover point is determined at which no shoot-through current occurs in the push-pull driver circuit.